**Verilog Thermostat Report**

# Problem Statement

The assignment asked for a rudimentary CPU thermostat module to be designed, implemented, and tested in Verilog. The thermostat will send out a signal to turn on the internal CPU fan when the temperature within the CPU exceeds a preset value. An appropriate testbench will be created to ensure correctness of the thermostat module, and to output the status of the simulation as it progresses.

# Approach

The thermostat module was designed to receive the preset and the current temperatures of the CPU via a 3-bit input, to allow for testing of all values within the given range (0-7) without superfluous memory usage. A 1-bit output wire was also decided upon, as the fan only needs to generate either a single “on” or a single “off” signal. The testbench functionality was placed within a separate module to improve readability of the thermostat functionality, and so that it would be easy to remove the testbench should this code ever theoretically be moved into live production. Verilog was decided as the proper implementation language for this simulation, with the vvp tool chosen as the simulation environment. Column headings were also added to the testbench output to improve readability of simulation statistics.

# Solution

The thermostat module was built first, with only a rudimentary testbench created to check for logical correctness during initial construction. The testbench was then expanded upon, to include all necessary functionality required for the assigned task. The thermostat itself performs a check if the current temperature is greater than the preset temperature, and if so, a signal is sent along a wire back to the it’s parent module informing the parent module that the fan should be turned on. A small amount of code within the testbench was reused to set the current temperature, as it felt excessive to write a complex concatenation statement for such a small range of values.

Attached is a screenshot (Figure 1) of the simulation source code (thermo.v) being compiled and then run, and includes the output of the testbench which gives statistics about the simulation. No errors were encountered during the simulation, and the output given was nominal. This task is therefore now complete, and is ready to be passed on to the theoretical client for approval.

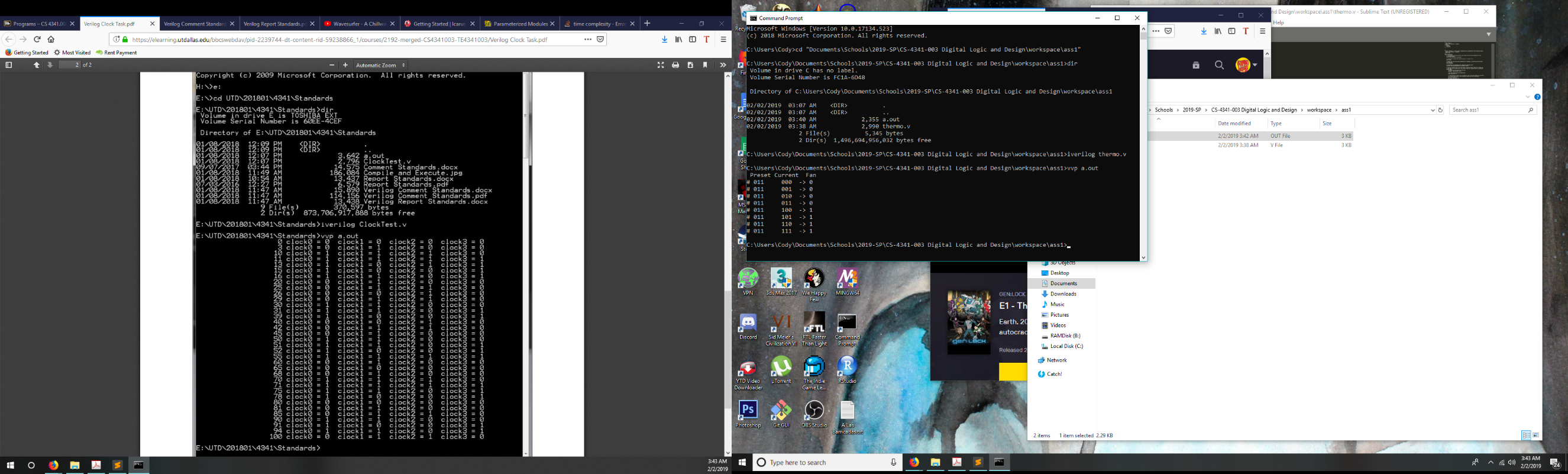
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Figure 1 – Output of testbench module while simulating the CPU thermostat